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**PC/FIP board 1Mbit/s
128K**

User Manual

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1. GENERAL PRESENTATION

1.1. INTRODUCTION

The PC/FIP board is a 8 bits ISA card to interface the WorldFIP (or FIP) field bus.

1.2. FUNCTIONALITY

The PC/FIP realizes an interface between an IBM-compatible personal computer and the WorldFIP (or FIP) field bus. The communication rate can be one of three standard rates of the WorldFIP (31,25 Kb/s, 1 M/s and 2.5 M/s) according to the board purchased.

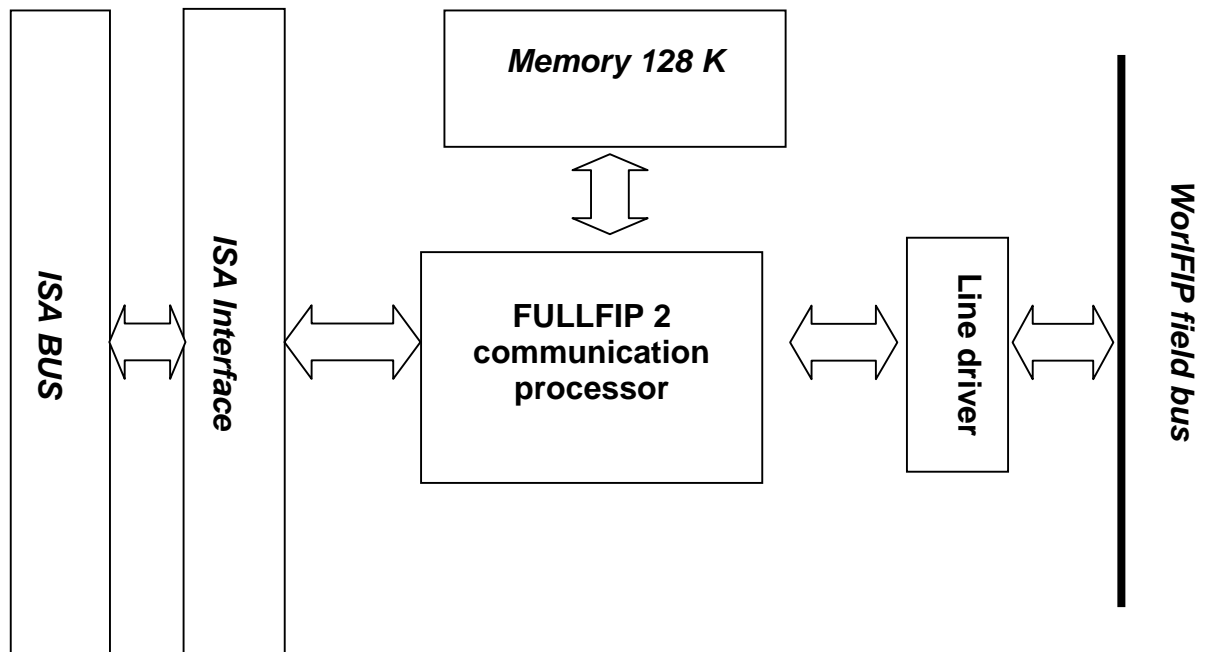
1.3. CHARACTERISTICS:

Memory: 128 K word (16 bits) memory for the communication processor FULLFIP2.

IO address range : From 0x200 to 0x3FF.

Interrupts available : IRQ3, IRQ4, IRQ5, IRQ6, IRQ7 and IRQ9.

1.4. ORGANIZATION OF THE PC/FIP BOARD



2. PC/FIP BOARD USAGE

2.1. BOARD ADDRESS SELECTION

The board address is selected using switches SW2 to SW4 (SW1 always set to 0). The address ranges from 200Hex to 3DF Hex.

Address PC	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
	0	0	1	SW 4	SW3	SW2	SW1	X	X	X	X	X
Address 200H	0	0	1	0	0	0	0	0	0	0	0	0
Address 3DFH	0	0	1	1	1	1	0	1	1	1	1	1

The A9 address line is set to "1" and the A10, A11 address lines are set to "0". The A0 to A4 address lines do not influence the address of the board, they are used for internal board addressing.

In general, only one switch is used to fix the board address. The default address is factory set at 280Hex. The four possible addresses are shown figure 2-1.



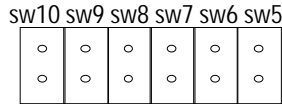
Figure 2-1 Board address selection

Another possible address (with two or three jumpers) are: 0X2C0, 0X340, 0X380, 0X3C0.

Attention: A5 (SW1) is used for the protection code in PC/FIP2.3. Please do not use the SW1.

2.2. BOARD INTERRUPT SELECTION

The FULLFIP2 circuit in the PC/FIP board can generate an interruption. This interruption can be one of the 6 interrupt lines available on the ISA bus. There is no factory setting for the interrupt line. The user can choose one of the following interrupt line : IRQ3, IRQ4, IRQ5, IRQ6, IRQ7, IRQ9 by using a jumper. (See figure 2-2).



IRQ 9 3 4 5 6 7

Figure 2-2 Board interruption selection

2.3. ACCESS TO INTERNAL REGISTERS

The A0 to A4 address lines can be used to select the FULLFIP2 operating mode according to table 2.1.

The FULLFIP2 must be in reset mode at least 1 µs to be properly reset.

A4	A3	A2	A1	A0	In write mode (Signal IOWCn=0)
0	1	0	0	1	FULLFIP on reset mode
0	1	0	0	0	FULLFIP on normal operation mode

Table 2-1

The FULLFIP2 registers are selected when the A3 and A4 address lines are zeroed. Lines A2 to A0 are used to select between the internal registers.

A4	A3	A2	A1	A0	Status register (Reading)	Command register (Writing)
0	0	0	0	0	U_STATE	U_COM
0	0	0	0	1	U_FLAGS	U_SWITCH
0	0	0	1	0	VAR_STATE	KEY_H("upper byte")
0	0	0	1	1	VAR_SIZE	KEY_L("lower byte")
0	0	1	0	0	unused	unused
0	0	1	1	0	unused	unused
0	0	1	1	1	File	File

Table 2-2

2.4. SWITCHES AND CONNECTORS

The switches and connectors position on the PC/FIP board is shown figure 2-3.

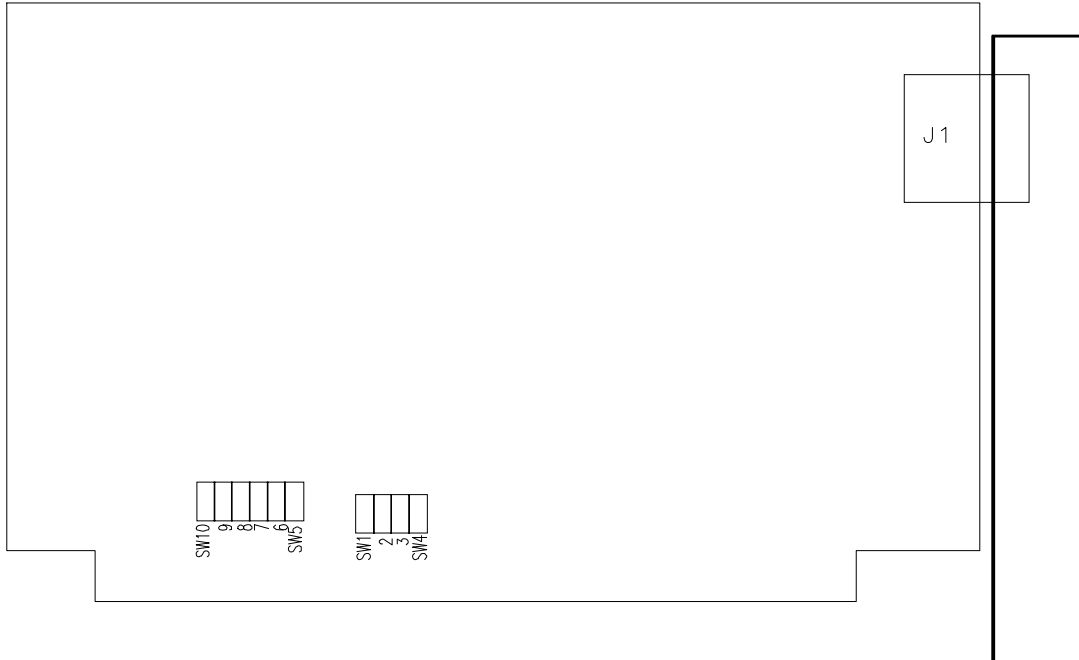


Figure 2-3 Position of switches on the PC/FIP board

The connection with the network WorldFIP (or FIP) is made through the J1 connector (Figure 2-4).

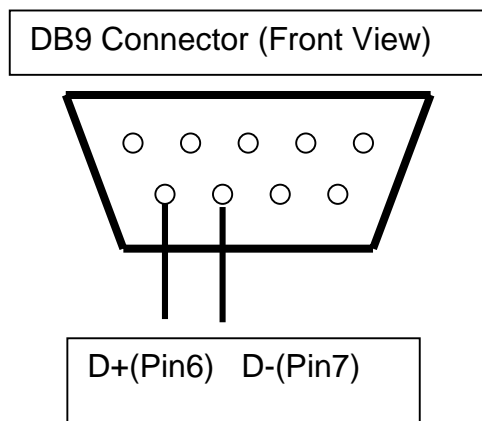


Figure 2-4 Connector J1